Development of 5.8GHz SiGe BiCMOS Direct Conversion Receivers

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Abstract — **We present the design, development and full characterization of two direct conversion receiver front-end architectures for IEEE802.11a application in IBM's SiGe BiCMOS technology. These approaches include: a) conventional 50Ω system, b) fully monolithic front-end. The developed ICs are targeted for the upper U-NII band at frequency range of 5.725-5.825 GHz and include a low noise amplifier (LNA), two mixers in quadrature, and a frequency divider. All of these circuits use fully monolithic implementation. The LNA provides a gain of 11 dB, noise figure of 4.4dB, IIP3 of –2dBm and occupies an area of 0.7mm X 0.7mm. A micromixer topology has been adopted in case of 50Ω system and provides 9.2dB gain, input matching of 16dB, double sideband noise figure of 19.5 dB, input 1 dB compression point of –3 dBm, IIP3 and IIP2 of +6 and +32 dBm respectively, dynamic DC offset of 1.6mV, and occupies an area of 1.6mm X 1mm. The fully integrated receiver utilizes single-ended Gilbert cell mixers, and occupies a compact area of 1.6mm X 1.3mm. It exhibits 20.2dB gain, input 1 dB compression point (input P1dB) of –15.5 dBm, input matching of 15 dB, IIP3 and IIP2 of –3 dBm and +31 dBm respectively, double sideband noise figure of 7.1 dB, dynamic DC offset of 1mV, and LO to RF leakage of 78 dB. The LNA draws 5.78mA from a 2.8V supply, both micromixers draw 10.3mA from 3.1V supply, both Gilbert cell mixers draw 12.71mA from a 3.75V supply, and the frequency divider draws 22mA from 3.75V supply. Two different system architectures are chosen for an architectural trade-off of direct conversion receivers at 5.8GHz. To the best of our knowledge, this work presents the first report of SiGe BiCMOS direct conversion receiver front-ends and their architectural trade-offs for the IEEE802.11a standard at 5.8GHz.**

I. Introduction

The proposition of high-speed (54Mbps or more) wireless LAN (WLAN) communication standards such as IEEE802.11a [1] has stimulated significant research activities in the recent past. This standard utilizes orthogonal frequency division multiplexing (OFDM) as the modulation scheme to provide robustness against intersymbol interference caused by multi-path effects. However, due to the high crest factor (also referred to as peak to average ratio) of the OFDM modulated signal waveform, the RF front end blocks require high linearity.

There have been reports of superheterodyne architectures for IEEE802.11a in the open literature [2,3]. However, the IEEE802.11a spectrum doesn't contain any information at zero frequency, thus facilitating the implementation of direct conversion architectures due to the "dc-free" modulation scheme. Advantages of the direct conversion receiver architecture over the superheterodyne include the elimination of bulky image reject filters, resulting in compact, low power and low cost solutions.

The SiGe process technology is quite attractive for next generation communication IC solutions [4] as it is capable of providing excellent RF performance in the front-end along with integration in the baseband, thereby favoring more monolithic integration for wireless applications. In this paper, we present two different direct conversion receiver front-end architectures and their realization in SiGe BiCMOS technology.

II. System Architectures

The 5-6 GHz band is divided into two parts. The lower U-NII band contains 8 carriers within 200MHz (5.15 – 5.35GHz) and the upper U-NII band contains 4 carriers within 100MHz (5.725-5.825GHz). Fig.s 1 and 2 show the front-end direct conversion architectures under consideration. Placement of the filter before the LNA provides a better system design for rejecting out of band interferers and facilitates comparison of both the system architectures. The dashed portions indicate the developed front-end circuit blocks. A differential configuration in the front-end mixers minimizes the effect of common mode noise and provides high IIP2 needed for direct conversion receivers.

The IEEE802.11a modulation uses 52 information carrying OFDM subchannels (each of which occupies 312.5 kHz), which are arranged symmetrically around a 53rd dc subchannel that contains no energy [1]. A system target of 10dB noise figure with 5dB of

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implementation margin has been set. I/Q imbalance is targeted for 0.4dB in amplitude and 3.7 degrees in phase. Input P1dB has been set at –16dBm.The overall front end gain can be set at 20 dB as a compromise between the overall system noise figure and linearity.

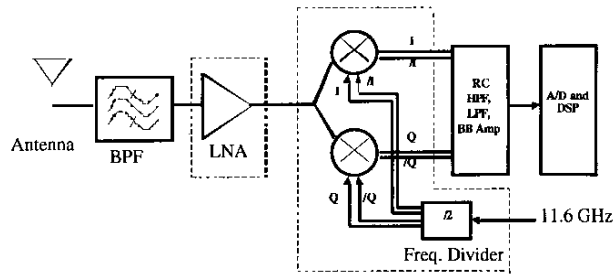

Fig.1. Conventional 50Ω receiver front-end architecture.

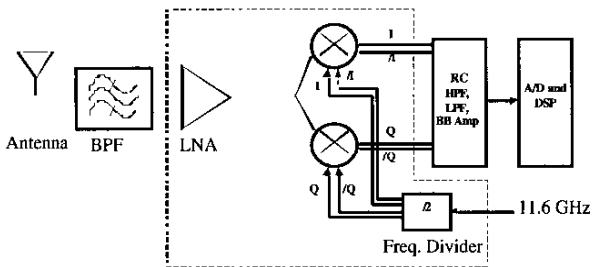

Fig.2. Fully integrated receiver front-end architecture.

III. Circuit Design

A. SiGe BiCMOS Process Technology

The developed ICs utilize IBM's BiCMOS6HP process technology. This process provides five metal layers with an additional thick metal layer (called analog metal, AM) for high Q inductor realization. The substrate resistivity is 10-20 Ω-cm and bipolar transistors with emitter widths of 0.32um, 0.44um and 0.8 um are available. The cutoff frequency (f_T) and maximum oscillation frequency (f_{MAX}) are 47 GHz and 60 GHz respectively. The NMOS and PMOS devices have 0.24um as nominal effective length. In addition, this process provides polysilicon and diffused resistors, high density MOS and high-Q metal insulator metal (MIM) capacitors and inductors.

B. LNA Design

The LNA utilizes a cascode topology with single-ended input and single-ended output. Bipolar transistors with lowest possible emitter width (0.32um) are used due to their superior performance in terms of lower noise (lowest r_{bb}). Use of cascode topology helps in isolating the input and output, thereby leading to separate optimization of input and output networks as well as providing an excellent LO to RF leakage performance for the integrated receiver. It also minimizes the effect of the Miller capacitor, thus favoring high frequency operation.

The size of the LNA input transistor has been chosen to be 50umX0.32um for noise figure optimization. Inductive degeneration has been used to achieve the required linearity performance as well as to facilitate input matching.

C. Mixer Design

The input stage of the micromixer [5] consists of quasi-balanced impedances containing a combination of inductor, resistor and a transistor in a diode-like configuration. The switching core is similar to a Gilbertcell like configuration. It provides a low input impedance stage, hence suitable for application in a conventional 50Ω system. The potential advantage of using a micromixer is its low power consumption and very high linearity performance.

An inductively-degenerated Gilbert cell with a bipolar differential pair at the input is used for each of the I/Q mixers for the fully integrated receiver, as the input stage usually exhibits higher impedance, hence better suited for on-chip integration. One end of the differential pair has been grounded for conversion from single-end to differential. These active mixers operate at very low LO power, resulting in the reduced possibility of LO to RF coupling through substrate and radiation.

Inductive degeneration helps achieve the linearity requirements while maintaining lower noise figure in the receiver. The operating frequency of the degeneration inductors should be less than: a) self resonating frequency of the inductors, b) resonating frequency of the network formed by the degeneration inductor and the base to emitter capacitance of the bipolar transistor at the input stage.

D. Frequency Divider

Direct conversion receivers are very sensitive to LO to RF interference, which results in DC offset. Hence, the input LO frequency is at a different value (usually 1/2X or 2X of the incoming RF frequency) to minimize LO to RF interference caused from the test fixtures and the probe cards to be used for testing. In our design, a 2X architecture based on a D Flip-flop based circuit has been used due to easy generation of quadrature signals (I, I/, Q, Q/). This architecture doesn't generate a frequency component at the subharmonic LO frequency, thereby improving LO to RF leakage performance. This circuit

takes an input signal at 11.6 GHz and generates the four differential outputs in quadrature phases at 5.8 GHz.

E. Layout Considerations

Due to the presence of both digital and high frequency RF circuits in the integrated receiver, the effect of digital noise has been minimized by an array of guard rings with substrate contacts. The power supplies for digital and analog circuits have also been kept separate for noise considerations. The symmetry of the RF signal lines in the layout is critical for minimizing I/Q imbalance. It is very critical to have symmetry for the clock distribution network in the DFF based frequency divider. A first level metal ring under the pads provides a robust on chip ground with several substrate contacts.

IV. Measurement Results And Discussions

Fig.s 3 and 4 show the pictures of the fabricated micromixer and receiver front-end IC respectively. Table I shows the performance summary of the fabricated ICs along with architectural trade-off.

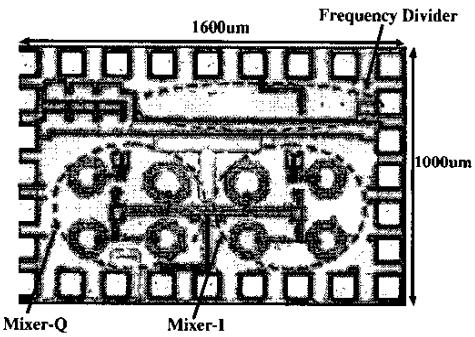

Fig.3. Die photograph of developed micromixer IC.

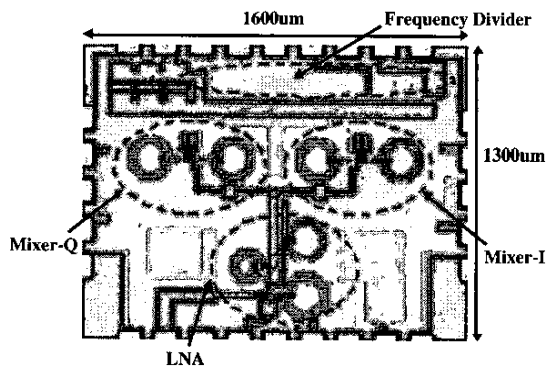

Fig.4. Die photograph of fully integrated receiver front-end (architecture-2).

For architecture-1, the overall performance is computed from the measurement results of the LNA and micromixer. The conventional 50Ω system (architecture-1) provides higher noise figure due to the high noise figure of the micromixer. However, the power dissipation is lower in the 50Ω architecture for similar linearity and gain performances. The developed ICs can be readily integrated with LTCC based front-end passives [6] for the entire front-end solution. The LNA exhibited an upward frequency shift (operates at 6.4 GHz) and higher noise figure (4.4 dB) compared to its simulated performances. The reasons for these can be attributed to the following facts: a) input on chip inductor is lossy, b) overall change of 10% in the inductance while in fabrication c) small inaccuracy of noise models at high frequencies d) additional coupling to the input inductor by other metal lines in the circuit. However, the LNA performs better in the fully integrated receiver IC and will be optimized in the next run. The I/Q imbalance is higher in measurement compared to expected performance from simulations, and is attributed to the unequal amounts of positive feedback caused from the on-chip ground in the cases of in-phase (I) and quadrature (Q) mixers. This is expected to be much lower in the next generation of the receiver by layout optimization. However, amplitude and phase balance specifications can be relaxed if the DSP compensates their distortion effects. In the integrated receiver (architecture-2), the LNA and mixer combination dissipates 64mW of power and the frequency divider operating at 11.6 GHz consumes 22mA of dc current from a 3.75V supply. The micromixers (I and Q) dissipates 32mW of power, and the LNA dissipates 16mW of power, giving rise to 48mW of power dissipation in LNA and Mixer circuits (architecture –1). However, 11.6 GHz is a fairly high input frequency for standard DFF based frequency dividers and a 1/2X architecture (input frequency of 2.9 GHz) shows potential for improving LO to RF isolation as well as power dissipation and can be adopted for the targeted application. This would be a better choice compared to the 2X architecture due to the proposed dc-free modulation scheme of IEEE802.11a.

Table-I: Performance summary of developed receiver (* denotes computed result from individual chip results, in case of architecture 1, which uses 50-ohm building blocks)

Performance	Inte-grated Rx	Micro mixer	LNA	LNA+ Micro-Mixer*
Gain (dB)	20.2	9.23	11	20.23
NF (dB)	7.1	19.5	4.4	9.89
ICP (dBm)	-15.5	-3	-10.4	-14.0
IIP3 (dBm)	-3	+6	-2	-6.76
IIP2 (dBm)	+31	+32	----	+21.0

Amplitude imbalance (dB)	0.9	0.2	---	
Phase imbalance (deg)	5	2.4	-----	
Power consumption (mW)	64	32	16	48
Input match (dB)	15	16	20	
LO power (dBm)	-10	-12	-----	
LO to RF leakage	78 dB	58 dB	-----	
Dynamic DC offset (mV)	<1	<1.6	-----	
Output match (dB)	--------	--------	12	

IV. Conclusions

We have presented design, development and full characterization for two different direct-conversion receiver front-ends for IEEE802.11a specification at 5.8GHz band, along with architectural issues and system considerations. Both the architectures use fully on chip implementation, meet the IEEE802.11a system linearity specification with 5 dB margin. Architecture-2 meets system NF specification (with a 3 dB LTCC filter loss) with 5dB margin whereas architecture 1 exhibits a higher system NF. The power dissipation is 48mW in LNA and mixer circuits for architecture-1 and 64mW in LNA and mixer circuits for the fully integrated receiver IC, 82mW in the frequency divider circuit, and area requirement is 1.6mm X 1.3mm for the fully integrated receiver front-end IC.

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